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(54) **Ferroelectric memory**

(57) An FeRAM in which sensing occurs without a dummy cell, using an unselected bitline as a reference. The read cycle includes two opposed pulses on the drive line: the first pulse provides a data-dependent signal out of the selected cell, and the second pulse restores the bit line to a level such that the DC bias voltage on an unselected bitline provides an optimal reference.
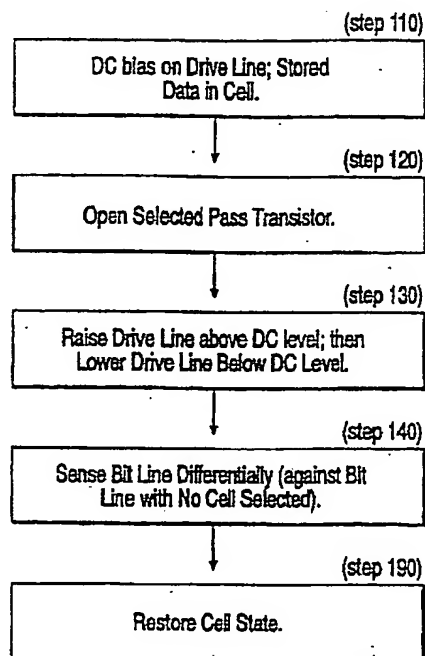
(step 110) DC bias on Drive Line; Stored Data in Cell.

(step 120) Open Selected Pass Transistor.

(step 130) Raise Drive Line above DC level; then Lower Drive Line Below DC Level.

(step 140) Sense Bit Line Differentially (against Bit Line with No Cell Selected).

(step 190) Restore Cell State.

FIG. 2

EP 0 928 004 A2

Description

[0001] The present invention relates particularly, but not exclusively, to Ferroelectric Random-Access Memories (FeRAMs), and to integrated circuits which include them.

[0002] Semiconductor memories normally use memory cells which are made as small as possible. As a result, the electrical signals which come out of these cells when the read operation is performed are extremely small. Thus, the sensing of semiconductor memories is a critical technology, which affects many other performance parameters. See B.Prince, Semiconductor Memories (2.ed 1991), which is hereby incorporated by reference. This is particularly true for ferroelectric memories.

[0003] One simple example of this is in the art of DRAM sensing. In a DRAM cell, information is stored by charging the cell capacitor to one of two voltages. By connecting the capacitor later to a bit line voltage which is intermediate between those two voltages, the stored charge, when dumped into one line of a bit line, will make the voltage on that bit line slightly different from that of a matched bit line. The sense amplifier amplifies this voltage difference to produce a large signal, which can be sensed by further amplifier stages (optional), and eventually by logic output stages.

[0004] In memory architectures generally, it is not only undesirable to have too little read margin (which can result in errors), but it is also undesirable to have too much read margin. (In this case it would be possible to shrink the cell further while still obtaining accuracy.) Thus, property designing the reference input for the sense amplifier is critically important to memory optimization. Where the profile of the possible output signals of the cell is relatively complex, as with ferroelectric memories for example, optimal tracking of the sense amplifier's reference is needed to provide the best possible margin of the sense amplifier. This translates directly into improvements in reliability and/or density.

[0005] Ferroelectric memories exploit the properties of ferroelectric materials, in which the induced electric field in the material is a nonlinear function of the applied voltage. See generally M.Lines and A.Glass, Principles and Applications of Ferroelectrics and Related Materials (1977), which is hereby incorporated by reference.

[0006] Ferroelectrics are analogous to ferromagnetic materials: just as the ferromagnetic material in a bar magnet can be permanently magnetized by applying a sufficiently strong magnetic field to it, and will thereafter act independently as a magnet, so a ferroelectric can acquire a fixed voltage gradient when a sufficiently strong electric field is applied to it.

[0007] This is useful in semiconductor memories, since ferroelectric materials have the potential to provide a non-volatile memory function. That is, after a ferroelectric material has been polarized in one direction, it will hold that polarization for a long time, and this pro-

vides non-volatile storage of information. (That is, the memory will retain its information even if it is not receiving any power supply voltage.) Ferroelectric random-access memories ("FeRAM"s) have therefore been a very active area of memory development. See generally, e.g., papers 25.1-25.7, 34.5, and 34.6 from the 1997 IEDM; all of which, and the references cited in them, are hereby incorporated by reference.

[0008] However, the sensing requirements of ferroelectric memories are difficult. Since the information in a ferroelectric memory cell is stored by polarization of the ferroelectric material (and not simply as charge), its read mechanism is actually quite different from that from a DRAM, SRAM, or floating-gate memory.

[0009] Figure 5 shows the "P/V" relation between stored charge density and applied voltage for a typical ferroelectric capacitor. Note that this curve has two values of charge for every value of voltage. Such curves are referred to as "hysteresis" curves. Depending on which polarization state the ferroelectric capacitor is in, a cell with stored data will either be at the "+Pr," point or at the "-Pr," point. ("Pr" is the spontaneous polarization density, and is measured in charge per unit area.) Note that the P/V hysteresis loop is nearly flat at these points, so a small change in voltage will not cause much charge transfer through the capacitor.)

[0010] Figure 3 shows a conventional two-transistor, two-capacitor type of FeRAM cell. In this case the unit cell $100'$, as indicated by a dotted line, includes two ferroelectric capacitors, each with its own pass transistor. The drive line DL_n is connected to drive one terminal of the ferroelectric capacitor of each capacitor pair, and the wordline WL_n is connected to open the pass transistors for both capacitors of a selected cell simultaneously. The two capacitor outputs then appear as a differential signal on the bit lines BL and $\overline{BL}$, and are amplified in a conventional differential sense amplifier 102. In such a cell, the capacitors of the cell pair are always written into opposite states, so that a relatively strong differential signal can always be obtained. However, this memory architecture is obviously not very area efficient.

[0011] Figure 4 shows a further prior art cell. In this case, only one capacitor is used for memory in each cell. As indicated by the dotted line, a unit cell $100'$ includes one transistor and one capacitor, and hence this is referred to as a "1T1C" cell. Again, the wordline WL_n is brought up to the positive logic level to turn on the pass transistor of the access cell. In this case the resulting output signal appears only as a single-ended signal on bitline BL_m (or $\overline{BL}_m$) The reference signal on the complementary bitline $\overline{BL}_m$ (or BL_m) is supplied by a dummy cell D_{mb} (or D_{ma}). The dummy cell D_{mb}, in this example, has a capacitor Cd whose lower terminal (as shown by the dashed connection) receives a signal equal to that on the drive line DL_n of the selected cells, and whose pass transistor is activated by the dummy word line WL_{db}. This provides a reference voltage on

the complementary bit line BL_m. However, this scheme is still quite difficult. The charge transfer through the ferroelectric capacitor of the selected cell, is dependent on its state of polarization and potentially different from that of a normal (paraelectric) capacitor like Cd.

[0012] Thus a disadvantage of the use of dummy cells in the prior art is that the dummy cell capacitor is not a ferroelectric capacitor, and thus its characteristics will not track those of a storage cell precisely. Moreover, the deposition and etch characteristics of the ferroelectric capacitor will not match those of a normal capacitor (which will typically have an oxide or oxynitride dielectric), so that process variation will not be identical between the two types of capacitor.

[0013] It is not practical to use a ferroelectric capacitor for the dummy cell, because complicated circuitry would be needed to drive the dummy cell properly. Moreover, the dummy cell consumes area.

[0014] The present application discloses a 1T1C ferroelectric memory architecture in which the read cycle includes two opposed pulses on the drive line: the first pulse provides a data-dependent signal out of the selected cell, and the second pulse restores the bit line to a level such that the DC bias voltage on an unselected bitline provides an optimal reference. (The second pulse also helps prepare the cell for restoration of its data state.) In some embodiments sensing occurs without a dummy cell, using an unselected bitline as a reference.

[0015] Advantages of the disclosed methods and structures include: A smaller cell area is realized in comparison with 2T2C cells; the disclosed scheme eliminates the complications of dummy cell schemes; a large voltage margin is available for accurate sensing; and good tolerance to power supply variations is achieved.

Brief Description of the Drawings

[0016] Embodiments in accordance with the invention will now be described by way of example only with reference to the accompanying drawings; wherein:

Figure 1A shows the cell connections of 1T1C FeRAM cell array.
Figure 1B is a timing diagram of the read operation, in the FeRAM array of Figure 1A.
Figure 2 is a flow chart of the steps of the FeRAM read operation.
Figure 3 shows a conventional two-transistor, two-capacitor type of FeRAM cell.
Figure 4 shows a prior art 1T1C FeRAM cell, which uses a dummy cell for sensing.
Figure 5 shows the relation between stored charge and applied voltage for a typical ferroelectric capacitor.
Figures 6A and 6B are an aligned pair of Figures which show the charge transfer through the cell of

Figure 1A during write and read operations.
Figures 7 and 8 show two different P/V trajectories on the hysteresis loop of Figure 5, corresponding to the read operations of Figure 1B.
Figures 9 and 10 show a more detailed plot of the P(V) relationships which underlie the trajectories shown in Figures 7 and 8.

[0017] The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

[0018] Figure 1A shows an innovative 1T1C FeRAM memory cell connection architecture, and Figure 1B shows the waveforms applied to and resulting from that cell in its two states.

[0019] In Figure 1A, each storage cell 100 is simply connected directly to a single one of the bit lines. In this example, the cell at array location (n,m) is connected to the m-th bit line BL_m, the nth drive line DL_n, and the nth word line WL_n. The sense amplifier 102 is connected to perform differential amplification between bit line BL_m and a complementary bit line $\overline{BL}_m$. Complementary bit line $\overline{BL}_m$ is connected to a cell which is connected to receive the (n+1)th drive line DL_{n+1} and the (n+1)th word line WL_{n+1}.

[0020] The present application discloses (in one class of embodiments) a 1T1C ferroelectric memory without a dummy cell. To make this work, the voltages of driveline, wordline, and bitline are operated in the following way, as shown in Figure 1B.

[0021] Initially, the bit lines and drive lines are all precharged to half the supply voltage (Vcc/2). (The DC bias level of Vcc/2 is chosen to minimize the stress on the components.) This is step 110 in the flowchart of Figure 2.)

[0022] The bitlines are then disconnected from power supply, and have a high impedance state.

[0023] When the word line goes high at time t_0 (step 120), the drive line is quickly thereafter driven with a fairly complex wave form as shown. (In FeRAMs as in DRAMs, the word line is typically driven with a boosted voltage, which is higher than the supply voltage.)

[0024] At time t_1, soon after the word line goes high, the drive line is driven up to V_{cc} (in this example).

[0025] If the cell is starting from the +Pr point, then at time t1 (as the curve BL(1), labelled "Bit Line for Stored One", shows) the bit line voltage will rise by a large margin over the DC bias level of Vcc/2.

[0026] If the cell is starting from the -Pr point, then at time t1 (as the curve BL(0), "Bit Line for Stored Zero", shows) the bit line voltage increases only slightly over

the DC bias level of Vcc/2.

[0027]   This is a destructive operation, in that the ferro-electric material no longer retains the data originally stored in the cell. However, this data is now shown by the bit line voltage.

[0028]   Thereafter (at **time t₂**) the drive line is driven down to a voltage which is below the DC bias voltage. (The drive line is driven down to Vcc/4 in this example, but other voltages below Vcc/2 can optionally be used.)

[0029]   As the curve BL(1) shows, the bitline voltage will preferably still be above the DC bias level in this case.

[0030]   As the curve BL(0) shows, the bitline voltage will fall well below the DC bias level in this case.

[0031]   In either case, the voltage which is applied at this stage will set the intrinsic polarization of the ferroe-lectric film to approximately zero, and thus this step pre-pares for the eventual writeback which restores the state of the cell. This completes step 130.

[0032]   Thereafter (at **time t₃**) the drive line is returned to its DC bias level (Vcc/2 in this example). The voltage of the bitline will be around +Pr/Cbit + Vcc/2 in the "1" case, where Cbit is the Bitline capacitance. (The bitline capacitance will typically be 7 or more times higher than the cell capacitance.) The voltage of the bitline will be around -Pr/Cbit+Vcc/2 in "0" case. As the curves of Fig-ure 1B show, the Vcc/2 level of an unselected bitline provides a reference level which is intermediate between these two states.

[0033]   At **time t4** the metastable positive-feedback sense amplifier is turned on, and the lines BL and B̄L̄ diverge to complementary logic levels (Vcc and ground) which indicate the stored data. (This specific example assumes a clocked sense amplifier, but of course a vari-ety of self-timing schemes for sensing can be used, as is well known by those skilled in the art.)

[0034]   Figures 6A and 6B are an aligned pair of Fig-ures which show the charge transfer through the cell of Figure 1A during write and read operations. In **Figure 6A**, the ferroelectric capacitor has initially been poled to the -Pr position. This is done, in this example, by apply-ing negative 5 volts for 40 microseconds. The second trace of Figure 6A shows the charge transfers appear-ing on the bit line as a result of this. Bit pulses Q1, Q2, and Q3 will appear on the bit line as a result of the drive pulses applied at times t1, t2, and t3. As may be seen from the voltage/time wave forms of Figure 1B, when the drive line voltage goes high at time t1, a substantial output pulse Q1 will be seen from the capacitor which has been charged to the +Pr position, while a much smaller output pulse Q1? will be seen from the capacitor which has been charged to the -Pr position. (This results from the trajectories Q1 and Q1? seen on the hysteresis loop of Figures 7 and 8.) Thereafter, when the secondary pulse is applied at time t2 a negative-going pulse Q2 will appear on the bit line in either case, and a further small positive pulse Q3 will appear at time t3 when the secondary pulse is ended. The sum of the

pulses Q1 (or Q1?) plus Q2 plus Q3 gives a net signal on the bit lines, which permits the correct read discrimi-nation as shown in Figure 1B. This net signal will now be further analyzed with reference to the traces of Figures 9 and 10.

[0035]   Figures 7 and 8 show how the charge and volt-age of an FeRAM cell evolve, in the hysteresis loop of Figure 5, depending on the starting state of the cell. Note that two trajectories are plotted. (In these curves, as in Figure 5, the specific example is a ferroelectric capacitor which includes 300 nm of lead zirconium titan-ate between iridium electrodes, and has a Pr value of 16.3 microCoulombs per square cm.) **Figure 8** shows the trajectory for a read operation on a cell which starts out in the +Pr polarization. In this case, the initial read operation at time t1, when the drive line goes high, increases the stored charge in the cell only along trajec-tory line P1, from +Pr to the absolute maximum charge at vertex B. This is a relatively small change, and hence the voltage change at one plate of the capacitor is cou-pled almost directly through to the other plate of the capacitor. This is why the bit line shows a large voltage change (in the trace BL(1), labelled "bit line for stored one" in Figure 1B). When the drive line thereafter drops below its DC bias level, the stored charge in the cell now shifts along trajectory Q2 back down to a point P. In this case, since a large change in the charge of the cell occurs for this voltage shift, the shift in the bit line volt-age is relatively small at time t2, at least in comparison to the large change in the drive line. Note that the increase in the drive line voltage at time t1 is less than the change in the drive line voltage at time t2; yet when one has been stored, the change in the bit line voltage is larger at time t1 than at time t2. By contrast, for a stored zero, the change in the bit line voltage is smaller at time t1 than at time t2.

[0036]   Thereafter, when the drive line voltage returns to its DC bias level, at time t3, the charge in this cell returns along trajectory Q3 to approximately a zero charge position.

[0037]   Note that this is not the end of the process. The reading process just described has destroyed the stored data in the cell, but has stored the cell data in the sense amplifier. The sense amplifier now is applying a voltage of either Vcc or zero to the bit line, and the dif-ference between this voltage and the drive line voltage (Vcc/2 in this example) will restore the cell to either +Pr or -Pr, at point A or A?. (Note that the transition to Vcc/4, at time t2, helps to prepare the cell for this write opera-tion.)

[0038]   Now refer to **Figure 7**. In this case, the initial state of the capacitor was at point A? rather than at point A, i.e., at charge density of -Pr rather than +Pr. In this case, the increase of the drive voltage at time t1 again drives the stored charge to state B, but the trajec-tory to get to point A? to B is trajectory Q1?. This trajec-tory has a much higher vertical distance, and this shows that a much larger amount of charge is transferred into

the cell capacitor for a zero cell than for a one cell, at time t1. This is why, in the curve BL(0) (labelled "bit line for stored zero"), the voltage increase in the bit line is much smaller at time t1 than in the curve for a stored one bit line: most of the change in drive voltage has gone to charging up the cell capacitor, and hence is not pumped through the cell. Thereafter, at time t2 and at time t3, the trajectories Q2 and Q3 are followed, just as in the example of Figure 8. However, the large difference in voltage change at time t1 permits the sense operation to proceed correctly. This Figure shows the sense amplifier as not started until after time t3, which is preferable to obtain the optimum sensing margin; but the relation between t3 and t4 does not have to be exactly as shown. (For example, self-timed timing relationships can optionally be used.)

[0039]   Figures 9 and 10 show a more detailed plot of the P(V) relationships which underlie the trajectories shown in Figures 7 and 8. **Figure 9** shows the case where the cell is initially in the -Pr position, that is where trajectory Q1? starts from point A?, and **Figure 10** shows the case where the cell is initially in the +Pr position, that is where trajectory Q1 starts from the point labeled A. Figure 10 shows how the charges have changed for a cell which begins from the +Pr position. In this case trajectories Q2 and Q3 may be seen to be identical as between Figures 9 and 10.

[0040]   To further explore the parameters of the described process, a series of experiments were run, using the same PZT cell structure whose P/V characteristics are illustrated in Figures 5, 7, and 8. In these experiments the magnitude of the secondary pulse, applied at time t2, was varied from -1V to -5V (after a first pulse, at about Vcc=5V, was applied at time t1). As these results show, the magnitude of the secondary pulse is relatively uncritical, and need not be precisely controlled.

[0041]   In an alternative embodiment, the voltage pulses can be inverted. In this case the drive line would be driven:

below the DC bias level (e.g. to ground rather than to Vcc) at time t1, to transfer a signal-dependent voltage onto the bitline; and

above the DC bias level (e.g. to 0.75*Vcc instead of 0.25*Vcc) at time t2, to cancel the polarization of the ferroelectric.

[0042]   In further alternative embodiments, it is contemplated that a voltage above Vcc or below ground could be used at time t1. This would be attractive if the ferroelectric film used has a hysteresis curve which (unlike that of Figure 5) does not converge within the voltage range available from the unboosted supply voltages. However, such boosting will tend to cause additional stress on components.

[0043]   It should also be noted that the use of bipolar drive pulses is NOT strictly limited to architectures with-

out a dummy cell. Even in architectures where a dummy cell is used to help sensing, the use of a complementary pair of pulses to restore a cell to an unpolarized state after a destructive read, is still expected to provide some advantages.

[0044]   According to various disclosed embodiments, there is provided: A method of reading a ferroelectric memory cell, comprising the steps of: (a.) providing a first pulse in a first direction onto a first terminal of a ferroelectric capacitor, to provide a charge output, at a second terminal of said capacitor, which indicates the poling of the dielectric in said capacitor; (b.) after said first pulse, providing a second pulse in a second direction, which is opposite said first direction, onto said first terminal; and after said step (b.), sensing the voltage of said second terminal.

[0045]   According to various disclosed embodiments, there is provided: A method of operating a ferroelectric memory, comprising the steps of: (a.) accessing a desired ferroelectric cell capacitor; (b.) providing a first pulse in a first direction onto a first terminal of said selected capacitor, to provide a charge output, at a second terminal of said capacitor, which indicates the poling of the dielectric in said capacitor; (c.) after said first pulse, providing a second pulse in a second direction, which is opposite said first direction, onto said first terminal; and (d.) differentially sensing the output voltage of a bit line which is connected to said second terminal, with respect to the output voltage of a bit line which is connected to another plurality of cells but not to any selected cell nor to any dummy cell.

[0046]   According to various disclosed embodiments, there is provided: A memory comprising: an array of ferroelectric memory cells, each comprising a ferroelectric capacitor, and a pass transistor having a gate connected to a respective word line, and having current-carrying terminals which are connected, in series with said capacitor, between a respective drive line connection and a respective bit line connection; and access circuitry which is connected to turn on said pass transistor of a selected cell, and to automatically apply two pulses of opposite signs to said drive line connection of said selected cell.

[0047]   According to various disclosed embodiments, there is provided: A memory comprising: an array of ferroelectric memory cells, each consisting of a single ferroelectric capacitor, and a pass transistor having a gate connected to a respective word line, and having current-carrying terminals which are connected, in series with said capacitor, between a respective drive line connection and a respective bit line connection; and access circuitry which is connected to turn on said pass transistor of a selected cell, and to automatically apply two pulses of opposite signs to said drive line connection of said selected cell; and a sense amplifier connected to sense the voltage on said bitline connection of said selected cell by a differential sensing operation against another bitline, without any dummy cell being activated.

[0048] As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given, but is only defined by the issued claims.

[0049] For example, the exact voltages used are not strictly necessary. The voltage Vcc/2 is selected to minimize stress, as is conventional, but of course other values can be used. Similarly, the exact value of Vcc/4 is not critical, but merely has to be somewhere between Vcc/2 and zero Volts.

[0050] It is also possible to use a more complex drive waveform, with additional pulses or delays added to the two drive pulses shown in the basic embodiment.

[0051] For another example, a variety of clocked or self-timing schemes for sensing can be used, as is well known by those skilled in the art.

[0052] The scope of the present disclosure includes any novel feature or combination of features disclosed therein either explicitly or implicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed by the present invention. The applicant hereby gives notice that new claims may be formulated to such features during the prosecution of this application or of any such further application derived therefrom. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the claims.

Claims

1. A method of reading a ferroelectric memory cell, comprising the steps of:

   (a.) providing a first pulse in a first direction onto a first terminal of a ferroelectric capacitor, to provide a charge output, at a second terminal of said capacitor, which indicates the poling of the dielectric in said capacitor;
   (b.) after said first pulse, providing a second pulse in a second direction, which is opposite said first direction, onto said first terminal; and
   (c.) after said step (b.), sensing the voltage of said second terminal.

2. The method of Claim 1, wherein said second pulse is smaller in magnitude than said first pulse.

3. The method of Claim 1 or Claim 2, wherein said second pulse is shorter in duration than said first pulse.

4. A method of operating a ferroelectric memory, comprising the steps of:

   (a.) accessing a desired ferroelectric cell capacitor;
   (b.) providing a first pulse in a first direction onto a first terminal of said selected capacitor, to provide a charge output, at a second terminal of said capacitor, which indicates the poling of the dielectric in said capacitor;
   (c.) after said first pulse, providing a second pulse in a second direction, which is opposite said first direction, onto said first terminal; and
   (d.) differentially sensing the output voltage of a bit line which is connected to said second terminal, with respect to the output voltage of a bit line which is connected to another plurality of cells but not to any selected cell nor to any dummy cell.

5. The method of Claim 4, wherein said second pulse is smaller in magnitude than said first pulse.

6. The method of Claim 4 or Claim 5, wherein said second pulse is shorter in duration than said first pulse.

7. A memory comprising:

   an array of ferroelectric memory cells, each comprising
   a ferroelectric capacitor, and
   a pass transistor having a gate connected to a respective word line, and having current-carrying terminals which are connected, in series with said capacitor, between a respective drive line connection and a respective bit line connection; and
   access circuitry which is connected to turn on said pass transistor of a selected cell, and to automatically apply two pulses of opposite signs to said drive line connection of said selected cell.

8. The memory of Claim 7, wherein said second pulse is smaller in magnitude than said first pulse.

9. The memory of Claim 7 or Claim 8, wherein said second pulse is shorter in duration than said first pulse.

10. An integrated circuit comprising a memory according to any of Claims 1 to 3 or Claims 7 to 9, or operable in accordance with any of Claims 4 to 6.
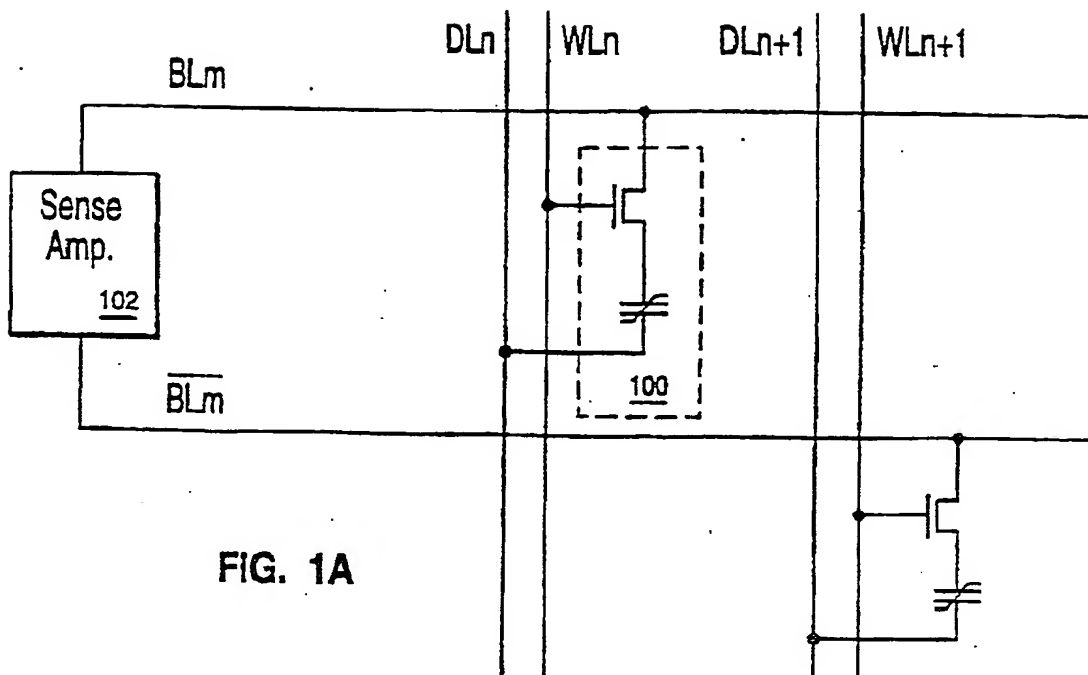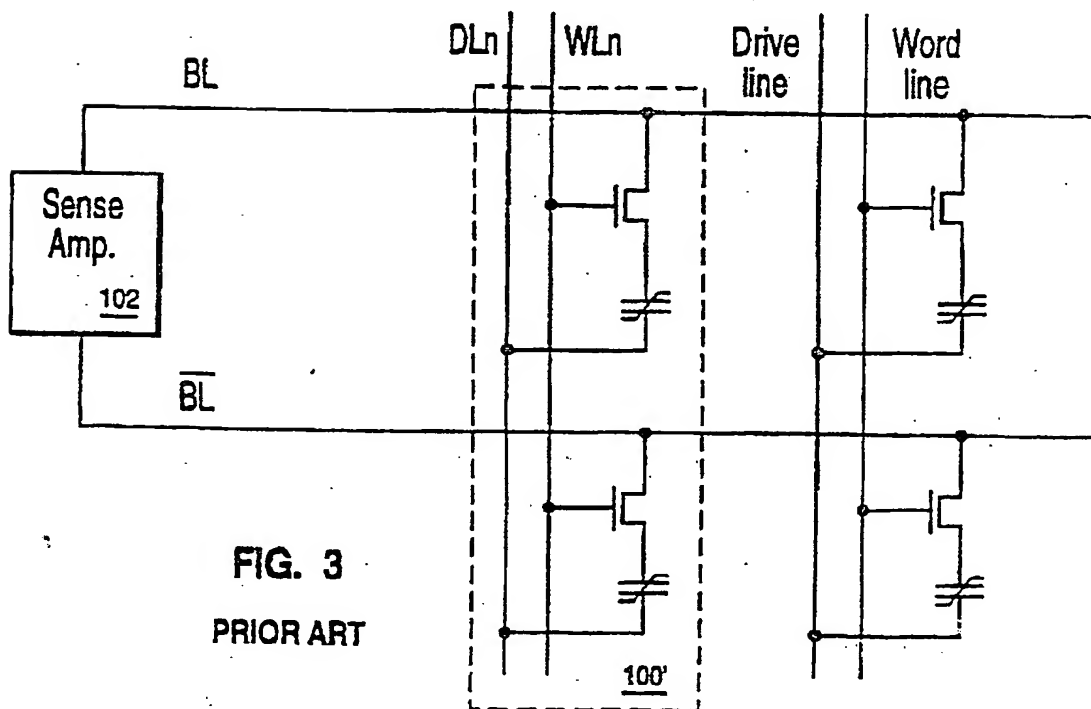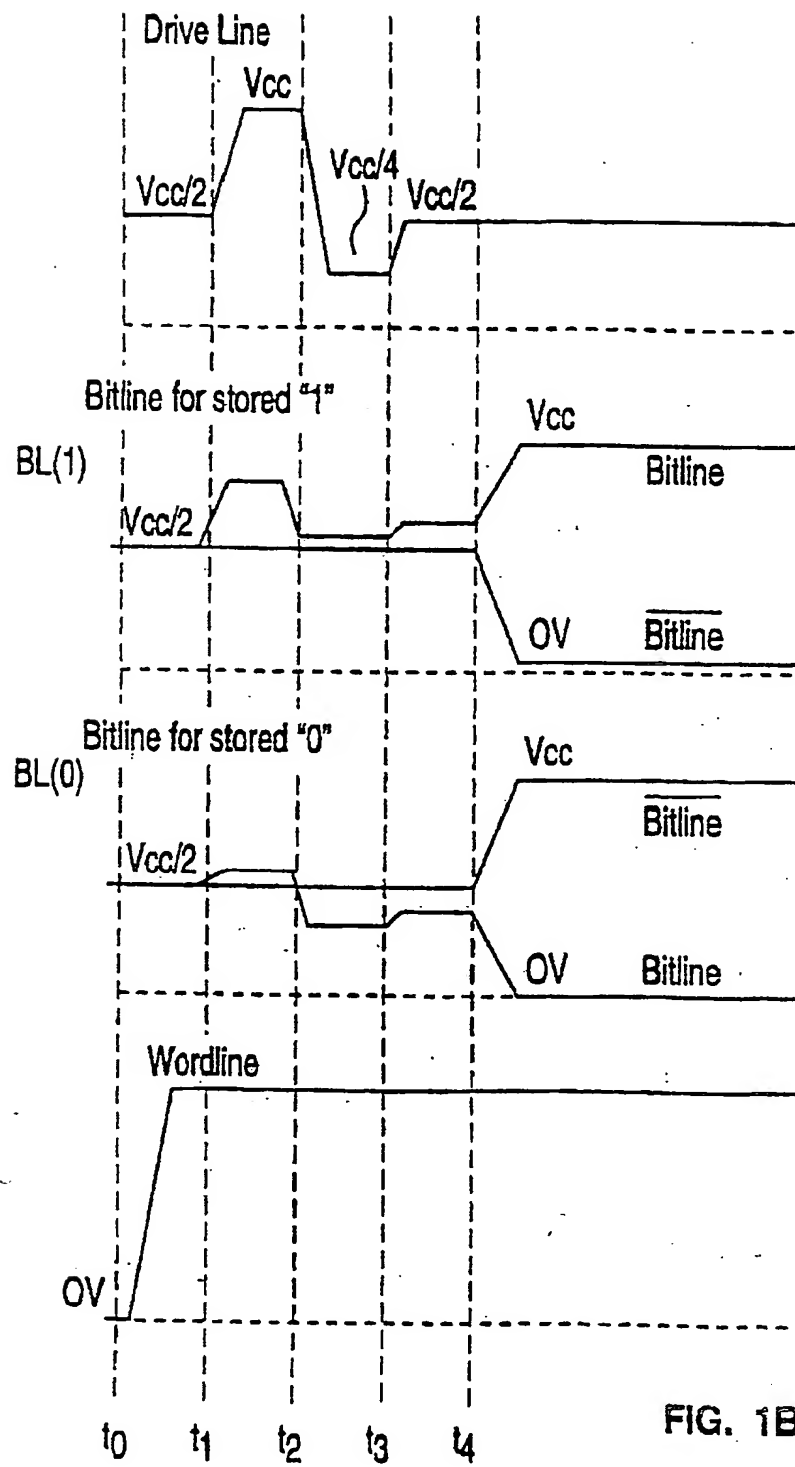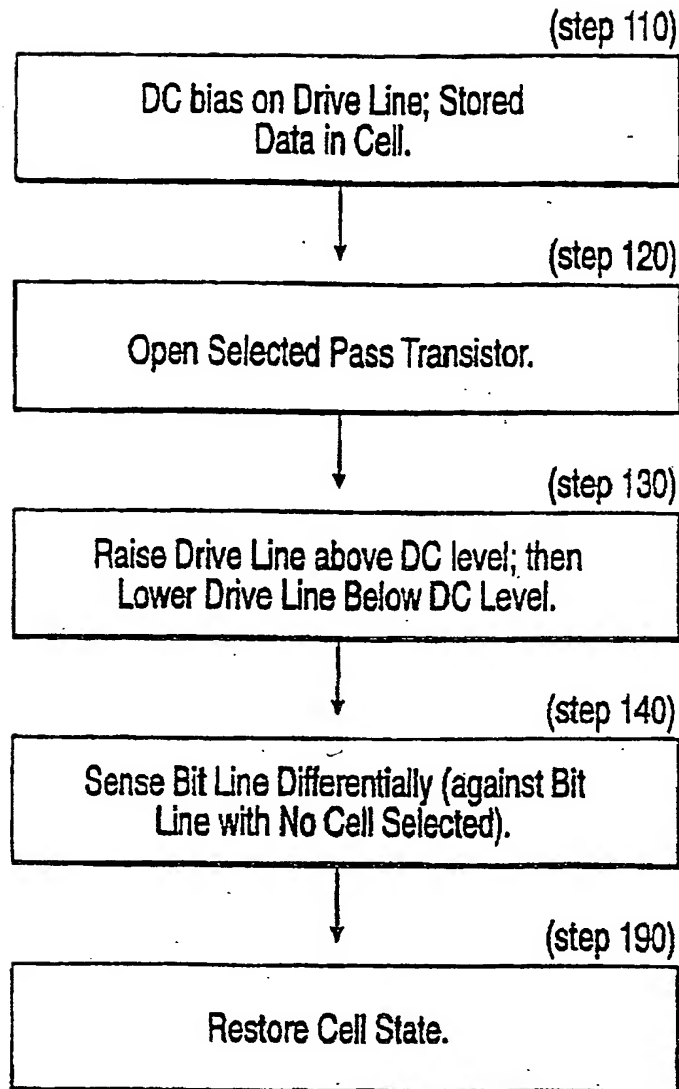
FIG. 1A

FIG. 3

PRIOR ART

FIG. 1B

(step 110)

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┌─────────────────────────────────┐
│   DC bias on Drive Line; Stored  │
│        Data in Cell.             │
└─────────────────────────────────┘
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(step 120)

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┌─────────────────────────────────┐
│   Open Selected Pass Transistor. │
└─────────────────────────────────┘
```

(step 130)

```
┌─────────────────────────────────┐
│ Raise Drive Line above DC level; then │
│   Lower Drive Line Below DC Level.    │
└─────────────────────────────────┘
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(step 140)

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┌─────────────────────────────────┐
│ Sense Bit Line Differentially (against Bit │
│     Line with No Cell Selected).           │
└─────────────────────────────────┘
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(step 190)

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┌─────────────────────────────────┐
│        Restore Cell State.       │
└─────────────────────────────────┘
```

FIG. 2

WLDb   WLDa   DLn   WLn   Drive line   Word line

BLm

Sense Amp. 102

Dma

BLm

100"

FIG. 4

PRIOR ART

Dmb

Cd

16.3 µ C/cm²

+Pr

-5V

Voltage [V]   +5V   V

-Pr

-16.3 µ C/cm²

FIG. 5

+5V | 1st pulse
80 μ sec

40 μ sec

OV

80 μ sec

Secondary pulse

-5V

Poling pulse
for -Pr position

varying -1.0V to -5.0V

$\Sigma Qn' = Q1' + Q2 + Q3$

Q1'

Q3

Q2

FIG. 6A

+5V | +5V

Poling pulse for
+Pr position

1st pulse
80 μ sec

OV

80 μ sec

40 μ sec

L

Secondary pulse

varying -1.0V to -5.0V

Q1

Q3

Q2

FIG. 6B

FIG. 7

FIG. 8

FIG. 9

FIG. 10